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(71) Applicant: SHARP KABUSHIKI KAISHA
22-22 Nagaike-cho
Abeno-ku
Osaka 545 (JP)

(72) Inventor: Kubota, Yasushi
5-1093-267, Asakuradainishi Sakurai-shi
Nara 633 (JP)
Inventor: Katoh, Ken-ichi
2613-1-1006, Ichinomoto-cho
Tenri-shi,
Nara 632 (JP)
Inventor: Yoneda, Hiroshi
5-1-2-303, Haginodai Ikoma-shi
Nara 630-02 (JP)

(74) Representative: White, Martin David et al
MARKS & CLERK,
57/60 Lincoln's Inn Fields
London WC2A 3LS (GB)

(54) A signal amplifier circuit and an image display device adopting the signal amplifier circuit.

(57) A signal amplifier circuit is provided with a buffer amplifier (1) and an adjusting circuit (2) for detecting a difference in voltage between a reference voltage (V_o) and an output voltage ($V_o + \Delta V$) of the buffer amplifier when the reference voltage (V_o) is inputted to the buffer amplifier (1) as an offset voltage, and for inputting a voltage obtained by subtracting the offset voltage (ΔV) from the voltage of an input signal so as to cancel out the offset voltage. An image display device of the present invention includes the above signal amplifier circuit. According to the above arrangement, the offset voltage (ΔV) can be cancelled out. Therefore, the signal amplifier circuit having a desirable buffer characteristic that a voltage having the same level as the voltage of the input signal can be outputted even if the offset voltage is generated in the buffer amplifier. By adopting the above signal amplifier circuit, an image display device which permits a high quality image display can be achieved.

FIG. 1

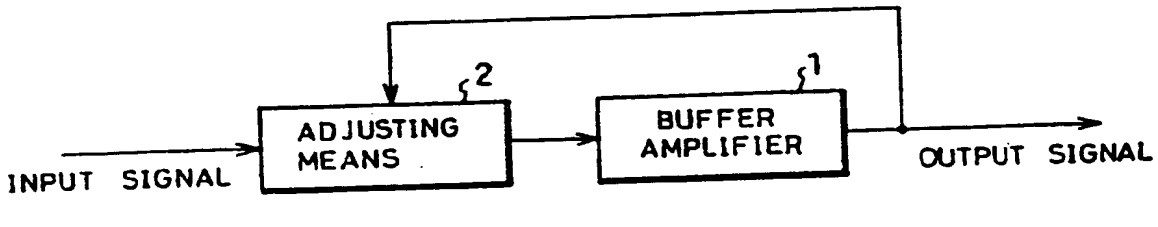

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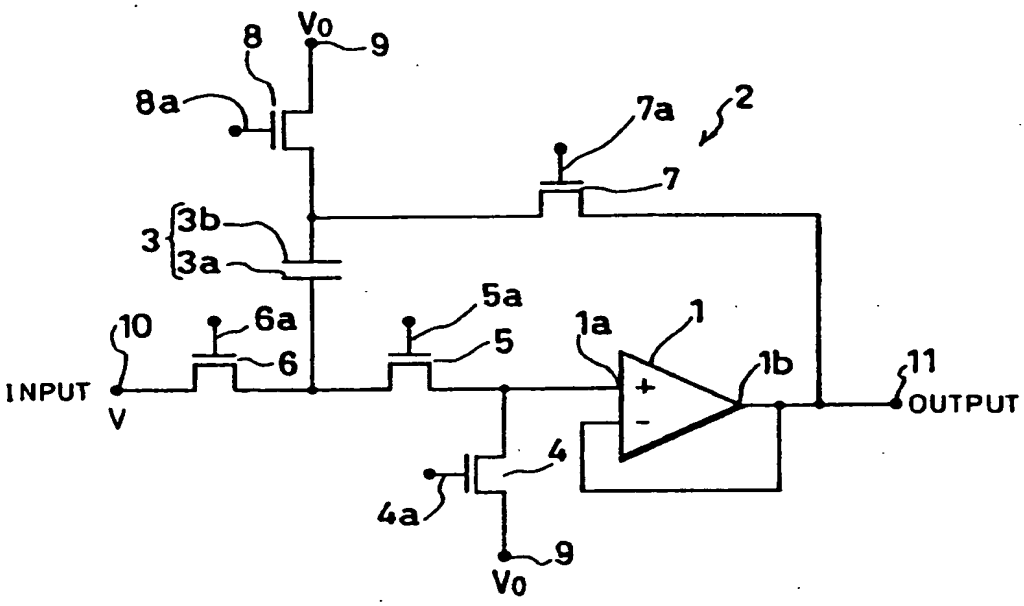
FIG.2



S_j can be ensured.

In the described liquid crystal display device of the active-matrix drive system, the FET 105 of the display cell C_{ij} (see Fig. 13) is formed using a thin film made of amorphous silicon formed on a transparent substrate, and drive circuits 101 and 102 are manufactured as separately provided ICs (integrated circuits). Recently, a monolithic system technology has been reported for forming the drive circuits 101 and 102 and the display 103 on a thin film made of polycrystalline silicon.

However, in the case of a transistor composed of the thin film made of polycrystalline silicon, since a particle diameter and a channel length of the transistor have the same order, properties such as a threshold voltage, mutual conductance, subthreshold coefficient, etc., differ for each transistor. Thus, in the case of manufacturing the buffer amplifier 115 (see Fig. 18 through Fig. 20), by the transistor made of the thin film made of polycrystalline silicon, the problem is presented in that an offset voltage is generated in the buffer amplifier 115. Here, the offset voltage is defined as a difference in voltage between the input voltage and the output voltage of the buffer amplifier 115.

The offset voltage differs for each buffer-amplifier 115, and this difference in the offset voltage may exceed 1 V. In the case of the liquid crystal display having a drive voltage (dynamic range) of 5 V, if a difference of offset voltages among buffer amplifiers 115 exceeds 1 V, a multiple gradation display of above 4 gradations cannot be carried out.

In order to counteract the above problem, the Japanese Laid-Open Patent Publication No. 1425941/1992 (Tokukaihei 4-142591) discloses a liquid crystal display device wherein a voltage for cancelling out the offset voltage is stored beforehand in the memory as adjusting data, and after adding the adjusting data to a video signal, the video signal is inputted into the drive circuit 101, thereby cancelling out the offset voltage.

However, when adopting the above liquid crystal display device, the following problems are newly raised: since a memory is required, a manufacturing cost goes up; and it takes time because an offset voltage is measured beforehand for each buffer amplifier 115 before being stored in the memory.

Moreover, since a Fermi level and a carrier mobility of a semiconductor has high temperature dependency, depending of an environmental temperature at which the liquid crystal display device is operated, the offset voltage may not be cancelled out. Furthermore, when using the transistor composed of the thin film made of polycrystalline silicon, the above properties greatly change as time passes because of the reasons that many localized levels exist on a crystal grain boundary and a gate dielectric film - polycrystalline silicon interface, and the polycrystalline silicon thin film is in a state of floating potential, thereby presenting the problem that cancelling out of the offset voltage cannot be ensured for a long period of time.

As described, the following problems still remain unsolved: the offset voltage generated in the buffer amplifier 115, especially, when the buffer amplifier 115 is manufactured using the transistor composed of the polycrystalline silicon thin film, a large offset voltage generated.

Furthermore, when adopting the buffer amplifiers 115 in which offset voltage generates, since the offset voltage differs for each buffer amplifier 115, a high quality image display cannot be achieved.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a signal amplifier circuit having a desirable buffer characteristic that a signal inputted thereto has the same voltage level as a signal outputted therefrom with a simple structure.

In order to achieve the above object, a signal amplifier circuit of the present invention is characterized by comprising:

a buffer amplifier; and

adjusting means for detecting a difference in voltage as an offset voltage between a reference voltage and an output voltage from the buffer amplifier when the reference voltage is inputted thereto, and for inputting a voltage obtained by subtracting the offset voltage from a voltage of an input signal into said buffer amplifier so as to cancel out the offset voltage.

According to the above arrangement, since the offset voltage can be cancelled out, even if the offset voltage generates in the buffer amplifier, a signal amplifier circuit having a desirable buffer characteristic that the signal inputted thereto has the same voltage level as the signal outputted therefrom can be achieved.

Another object of the present invention is to provide an image display device which enables a high quality image display.

In order to achieve the above object, an image display device of the present invention which comprises:

a buffer amplifier;

a display composed of display cells arranged so as to form a matrix;

a first drive circuit for sampling a video signal so as to send a voltage obtained by sampling as data over a data signal line; and

a second drive circuit for selecting a scanning signal line in order so as to send data on the data signal line to each display cell,

DESCRIPTION OF THE EMBODIMENTS

The following description will discuss embodiments of the present invention with reference to Fig. 1 through Fig. 11 and Fig. 21.

As shown in Fig. 1, a signal amplifier circuit in accordance with the present embodiment is provided with a buffer amplifier 1 and adjusting means 2 for cancelling out an offset voltage ΔV generated in the buffer amplifier 1.

The adjusting means 2 inputs a reference voltage V_0 to the buffer amplifier 1 and detects a difference between an output voltage ($V_0 + \Delta V$) of the buffer amplifier 1 and a reference voltage V_0 as an offset voltage ΔV. Then, the adjusting means 2 inputs a voltage ($V - \Delta V$) obtained by subtracting the offset voltage $^{\Delta}V$ from the voltage V of the input signal into the buffer amplifier 1.

When the voltage ($V - \Delta V$) is inputted to the buffer amplifier 1, a voltage ($V - \Delta V + \Delta V$) is outputted. Namely, the offset voltage ΔV is cancelled out, and the voltage V is outputted. According to the signal amplifier circuit of the present embodiment, even if the offset voltage ΔV is generated in the buffer amplifier 1, a desirable buffer characteristic that a signal outputted therefrom has the same voltage level as a signal inputted thereto can be achieved.

Therefore, even when the buffer amplifier 1 is manufactured using a transistor composed of a polycrystalline semiconductor or amorphous semiconductor, a signal amplifier circuit having a desirable buffer characteristic can be achieved.

It may be arranged such that the adjusting means 2 detects the offset voltage ΔV when the signal amplifier circuit starts operating. However, in the case where an input signal is inputted in synchronous with a clock signal, a detection of the offset voltage ΔV is preferably carried out at every clock.

In the above arrangement where the offset voltage ΔV is cancelled out at every clock, even if the offset voltage ΔV changes due to a change in the environment under which the signal amplifier circuit operates (for example, a change in temperature) or due to a change in properties of the signal amplifier circuit as time passes, cancelling out of the offset voltage ΔV can be always ensured.

The first example of the signal amplifier circuit will be explained below in reference to Fig. 2.

The signal amplifier circuit is composed of a buffer amplifier 1 and the adjusting means 2. The adjusting means 2 is composed of a condenser 3 (first condenser) and switching elements 4-8 (first - fifth switching elements).

An input terminal 1a of the buffer amplifier 1 is connected to an input terminal 9 of a reference voltage V_0 via the switching element 4. The input terminal 1a of the buffer amplifier 1 is also connected to one electrode 3a of the condenser 3 via the switching element 5. The electrode 3a is connected to an input terminal 10 of the signal amplifier circuit via the switching element 6. The other electrode 3b of the condenser 3 is connected to an output terminal 1b of the buffer amplifier 1 via the switching element 7. The electrode 3b of the condenser 3 is also connected to an input terminal 9 via the switching element 8.

In order to stabilize a signal level, another condenser of a small capacity may be added to the input terminal 1a of the buffer amplifier 1. This is effective if respective parasitic capacities of the buffer amplifier 1 and switching elements 4 and 5 and the capacity of wires used in connecting the above components are not sufficient for stabilizing the signal level.

Hereinafter, it is assumed that the buffer amplifier 1 always generates a constant offset voltage ΔV as long as the level of an input signal falls within a predetermined range.

The switching elements 4-8 are respectively controlled by control signals 4a - 8a from the control means (not shown) according to a timing chart of Fig. 3.

It is shown in Fig. 3 that respective rises and falls of control signals 4a-8a completely coincide in a time period of $t_1 - t_5$. In practice, however, when respective levels of the control signals 4a-8a change, finite time (transition time) is required. Therefore, in order to cancel out an offset voltage ΔV accurately, it is necessary to prevent an interference by a transient signal generated at respective rises and falls of the control signals 4a-8a. For the reason above, it is preferably prevent an interference occurred at rises and falls of the control signals 4a-8a, for example, by delaying a rise of one of the control signals 4a-8a. Additionally, the control signals 4a-8a are applicable to the case where a N-channel MOS transistor is adopted as switching elements 4-8. However, when P-channel MOS transistor is adopted as switching elements 4-8, the phase of the control signals 4a-8a should be reversed. The above features are also true of a timing chart to be described later.

At t_1, control signals 4a, 5a and 7a are High level and control signals 6a and 8a are Low level, and thus switching elements 4, 5 and 7 are set ON and switching elements 6 and 8 are set OFF.

Therefore, the reference voltage V_0 is applied to the input terminal 1a of the buffer amplifier 1 through a switching element 4; in the meantime, it is applied to the electrode 3a of the condenser 3 through the switching element 5. The output voltage ($V_0 + \Delta V$) of the buffer amplifier 1 is applied to the electrode 3b of the condenser 3 through the switching element 7.

element 7. As a result, the condenser 17 is charged, and the potential of the electrode 3b of the condenser 3 becomes the output voltage (V_o + ΔV) of the buffer amplifier 1 when the reference voltage V_o is inputted. Then, the offset voltage ΔV is cancelled out using the voltage (V_o + ΔV) held in the condenser 17. Other than the above, the signal amplifier circuit of this example has the same configuration as the previous example.

In the signal amplifier circuit of this example, a time required for cancelling the offset voltage ΔV is (t_3 - t_1) shown in Fig. 9.

In the present embodiment, the reference voltage V_o is not specified as long as it falls within a range where the linearity of the buffer amplifier 1 is ensured. However, it is preferably set to a mid-value of a range of the input signal level of the signal amplifier circuit. As a result, the non-linearity of the buffer amplifier 1 can be minimized, thereby achieving an accurate signal amplifier circuit. Moreover, because a change in the output from the buffer amplifier 1 in a period required for cancelling out the offset voltage V_o can be suppressed evenly, the time required for it can be reduced. Furthermore, since current applied to the condensers 3, 16 and 17 or switching elements 4-8, 14, 15, 21 and 22 can be made smaller, a transient generated at respective rises and falls of the control signals 4a-8a can be suppressed.

A constant voltage V_1 to be applied to an electrode of the condenser 16 on the other side of the switching element 15 and a constant voltage V_1 to be applied to an electrode of the condenser 17 on the other side of the switching element 7 are not specified as long as they are constant. However, for the reasons above, the constant voltage V_1 and V_2 are preferably set to a mid-value of a range of the input signal level of the signal amplifier circuit.

In the above examples, respective internal capacities of switching elements 4, 5... and parasitic capacities of wires are preferably set significantly smaller than the electrostatic capacity of the condenser 3 in order to surely cancel out the offset voltage ΔV.

For example, for each switching element 4, 5 ..., N-channel or P-channel MOS (metal oxide semiconductor) transistor, or a complementary MOS (CMOS) transistor switch composed of a N-channel MOS and a P-channel MOS connected in parallel may be used.

The N-channel MOS transistor and the P-channel MOS transistor, respective waveforms of gate electrodes when opening and closing a switch have phases opposite to one another. Therefore, by adopting the CMOS transistor switch, a potential shift due to the parasitic capacity between the gate electrode and the source electrode can be eliminated. For the above reason, a more accurate signal amplifier circuit can be achieved by adopting the CMOS transistor switch.

In the above preferred examples, the condensers 3, 16 and 17 are used for holding a voltage. However, the present invention is not limited to this. For example, other kinds of analog memory means or digital memory means of a plurality of bits may be used. For the analog memory means, a condenser provided between metal wiring layers or between the metal wiring layer and a semiconductor layer may be used. For the digital memory means, other than those having the same configurations as the analog memory means (condenser), a logic circuit such as a flip-flop may be used.

As an application example of the signal amplifier circuit, a liquid crystal display of an active-matrix drive system adopting the signal amplifier circuit will be explained below.

As shown in Fig. 10, the liquid display is composed of drive circuits 51 and 52 (first and second drive means), a display 53 composed of display cells arranged so as to form a matrix and a timing signal generating circuit 54 (i.e., a clock signal and control signals 5a, 6a, ...) provided for controlling the drive circuits 51 and 52. The timing signal generating circuit 54 may be formed on the substrate whereon the display 53 is formed or on a substrate separately provided.

The drive circuit 51 samples a video signal in synchronous with the timing signal and sends a voltage obtained by sampling as data over the data signal line S_j (Fig. 11). The drive circuit 52 selects a scanning signal line G_i in order (Fig. 12), and data on the data signal line S_j is sent to a display cell of the display 53.

As shown in Fig. 11, an analog driver of linear sequential drive system which serves as the drive circuit 51 is composed of a shift register 57, a plurality of latches 58, a plurality of switching circuits 59, a plurality of condensers 60 and a plurality of signal amplifier circuits 61. Here, it is possible to omit latches 58.

As shown in Fig. 21, the shift register 57 sends a signal over latches 58 in order in synchronous with a clock signal. Each latch 58 holds a signal from the shift register 57 and shifts a signal level if necessary. Each switching circuit 59 is set ON by a signal from the latch 58, and the level of a video signal at that time is sampled to the condenser 60 as data. In the described manner, data of an effective horizontal scanning period, i.e., data of the same number as the number of picture elements in a lateral direction are held in a plurality of condensers 60 respectively.

As described, the signal amplifier circuit 61 is provided with the buffer amplifier 1 and the adjusting means 2 for cancelling out an offset voltage ΔV

ΔV is cancelled out by the adjusting means 2 at every clock.

According to the arrangement of the second amplifier circuit, the following effect can be achieved in addition to the effect attained from the first signal amplifier circuit. By cancelling out the offset voltage ΔV at every clock, even if the offset voltage ΔV changes due to a change in the environment under which the signal amplifier circuit is operated (for example, change in temperature) or due to a change in characteristic of the signal amplifier circuit as time passes, cancelling out of the offset voltage ΔV can be always ensured.

The third signal amplifier circuit having the structure of the second signal amplifier circuit is arranged such that the adjusting means 2 is composed of a condenser 3 and switching elements 4-8, and that an input terminal 1a of the buffer amplifier 1 is connected to an input terminal 9 of a reference voltage V_0 through the switching element 4 and is also connected to one electrode 3a of the condenser 3 through the switching element 5. The third signal amplifier circuit is further arranged such that the electrode 3a of the condenser 3 is connected to an input terminal 10 of the input signal through the switching element 6, and the other electrode 3b of the condenser 3 is connected to an output terminal 1b of the buffer amplifier 1 through the switching element 7 and is connected to the input terminal 9 of the reference voltage V_0 through the switching element 8.

The third signal amplifier circuit enables a reduced number of components in addition to the effect of the second signal amplifier circuit.

The fourth signal amplifier circuit having the structure of the second signal amplifier circuit, the adjusting means 2 is composed of condensers 3 and 16 and switching elements 5-8, 14 and 15, and the input terminal 1a of the buffer amplifier 1 is connected to the electrode 3a of the condenser 3 through the switching element 5 and is connected to a constant voltage terminal through the switching element 15 and the condenser 16. The fourth signal amplifier circuit is further arranged such that the electrode 3a of the condenser 3 is connected to the input terminal 10 of the input signal through the switching element 6 and is connected to the input terminal 9 of the reference voltage V_0 through the switching element 14, and that the other electrode 3b of the condenser 3 is connected to the output terminal 1b of the buffer amplifier 1 through the switching element 7 and is connected to the input terminal 9 of the reference voltage V_0 through the switching element 8.

The fourth signal amplifier circuit enables a reduced number of components in addition to the effect of the second signal amplifier circuit.

The fifth signal amplifier circuit having the structure of the second signal amplifier circuit is arranged such that the adjusting means 2 is composed of condensers 3 and 17 and switching elements 4, 6-8, and the input terminal 1a of the buffer amplifier 1 is connected to the input terminal 9 of the reference voltage V_0 through the switching element 4 and is connected the electrode 3a of the condenser 3. The fifth signal amplifier circuit is further arranged such that the electrode 3a of the condenser 3 is connected to the input terminal 10 of the input signal through the switching element 6, and the other electrode 1b of the condenser 3 is connected to the other output terminal 1b of the buffer amplifier 1 through the switching element 7 and is connected to the input terminal 9 of the reference voltage V_0 through the switching element 8. The other electrode 3b of the condenser 3 is also connected to the constant voltage terminal through the condenser 17.

The fifth signal amplifier circuit enables a reduced number of components in addition to the effect of the second signal amplifier circuit.

The sixth signal amplifier circuit having the structure of the first, second, third, fourth or fifth signal amplifier circuit is arranged such that a switching element 21 is provided for applying the reference voltage V_0 to the output terminal 1b of the buffer amplifier 1.

The sixth signal amplifier circuit permits a load of the buffer amplifier 1 to be reduced in addition to the effect obtained from the effect of the first, second, third, fourth or fifth signal amplifier circuit. Therefore, a time required for cancelling out the offset voltage ΔV can be shortened.

The seventh signal amplifier circuit having the arrangement of the first, second, third, fourth or fifth signal amplifier circuit is arranged such that a switching element 22 for separating the buffer amplifier 1 from an external load is provided.

The seventh signal amplifier circuit permits a load of the buffer amplifier 1 to be reduced in addition to the effect of the first, second, third, fourth or fifth signal amplifier circuit. Therefore, a time required for cancelling out an offset voltage ΔV can be reduced.

The eighth signal amplifier circuit having the structure of the third signal amplifier circuit is arranged such that at least one of the switching elements 4-8 is a complementary MOS transistor switch.

The eighth signal amplifier circuit permits a higher accuracy compared with the signal amplifier circuit adopting a N-channel or P-channel MOS transistor switch, in addition to the effect of the third signal amplifier circuit.

The ninth signal amplifier circuit having the structure of the fourth signal amplifier circuit is

Claims

1. A signal amplifier circuit comprising:
a buffer amplifier; and
adjusting means for detecting a difference in voltage as an offset voltage between a reference voltage and an output voltage from said buffer amplifier when the reference voltage is inputted thereto and for inputting a voltage obtained by subtracting the offset voltage from a voltage of an input signal into said buffer amplifier so as to cancel out the offset voltage.

2. The signal amplifier circuit as set forth in claim 1, wherein:
the input signal is inputted in synchronous with a clock, and the offset voltage is cancelled out every clock by said adjusting means.

3. The signal amplifier circuit as set forth in claim 1 or 2, wherein:
said adjusting means is composed of a first condenser and first through fifth switching elements;
an input terminal of said buffer amplifier is connected to an input terminal of the reference voltage through the first switching element and to one electrode of the first condenser through the second switching element;
said one electrode of the first condenser is connected to an input terminal of the input signal through the third switching element; and
the other electrode of the first condenser is connected to an output terminal of said buffer amplifier through the fourth switching element and to the input terminal of the reference voltage through the fifth switching element.

4. The signal amplifier circuit as set forth in claim 1 or 2, wherein:
said adjusting means is composed of first and second condensers and second through seventh switching elements;
an input terminal of said buffer amplifier is connected to one electrode of the first condenser through the second switching element and to a terminal of a constant voltage through the seventh switching element and the second condenser;
said one electrode of the first condenser is connected to an input terminal of an input signal through the third switching element and to an input terminal of the reference voltage through the sixth switching element; and
the other electrode of the first condenser is connected to an output terminal of said buffer amplifier through the fourth switching element and to the input terminal of the reference voltage through the fifth switching element.

5. The signal amplifier circuit as set forth in claim 1 or 2, wherein:
said adjusting means is composed of first and third condensers and first, third, fourth and fifth switching elements;
an input terminal of said buffer amplifier is connected to an input terminal of the reference voltage through the first switching element and to one electrode of the first condenser;
said one electrode of said first condenser is connected to an input terminal of an input signal through the third switching element;
the other electrode of the first condenser is connected to an output terminal of said buffer amplifier through the fourth switching element and to an input terminal of the reference voltage through the fifth switching element; and
the other electrode of the first condenser is connected to a terminal of a constant voltage through the third condenser.

6. The signal amplifier circuit as set forth in claim 1, 2, 3, 4 or 5, wherein:
an eighth switching element for applying the reference voltage to an output from said buffer amplifier is provided.

7. The signal amplifier circuit as set forth in claim 1, 2, 3, 4 or 5, wherein:
a ninth switching element for separating said buffer amplifier from an external load is provided.

8. The signal amplifier circuit as set forth in claim 3, 4 or 5, wherein:
at least one of the switching elements is a complementary MOS transistor switch. switch.

9. An image display device comprising:
a display composed of display cells arranged so as to form a matrix;
a first drive circuit for sampling a video signal so as to send a voltage obtained as data by sampling over a data signal line; and
a second drive circuit for selecting a scanning signal line in order so as to send data on the data signal line to each display cell,
wherein said first drive circuit includes:
a shift register;
switching circuits in the same number as the number of display cells in a lateral direction;
sampling-use condensers in the same

16. The image display device as set forth in claim 11, 12 or 13 wherein:
at least one of the switching elements is a complementary MOS transistor switch.

17. The image display device as set forth in claim 9 , wherein:
said display cells and said first drive circuit are formed on the same substrate.

18. The image display device as set forth in claim 17, wherein said substrate comprises:
a transparent substrate having formed thereon an amorphous silicon thin film or polycrystalline silicon thin film.

19. The image display device as set forth in claim 9, 17 or 18, wherein:
a level of the video signal is consecutive.

20. The image display device as set forth in claim 9, 17 or 18, wherein:
the video signal is discrete having at least four levels.

21. The image display device as set forth in claim 9, 17, 18, 19, 20, 21 or 22, wherein:
each display cell includes a liquid crystal display element.

22. The signal amplifier circuit as set forth in claim 1, wherein said adjusting means includes:
a first condenser; and
switching means which applies an output voltage from said buffer amplifier when a reference voltage is inputted thereto to a first electrode of a condenser and applying a voltage of an input signal to a second electrode of the condenser, and thereafter, applies the reference voltage to the first electrode of the condenser and connects the second electrode to said buffer amplifier.

FIG.2

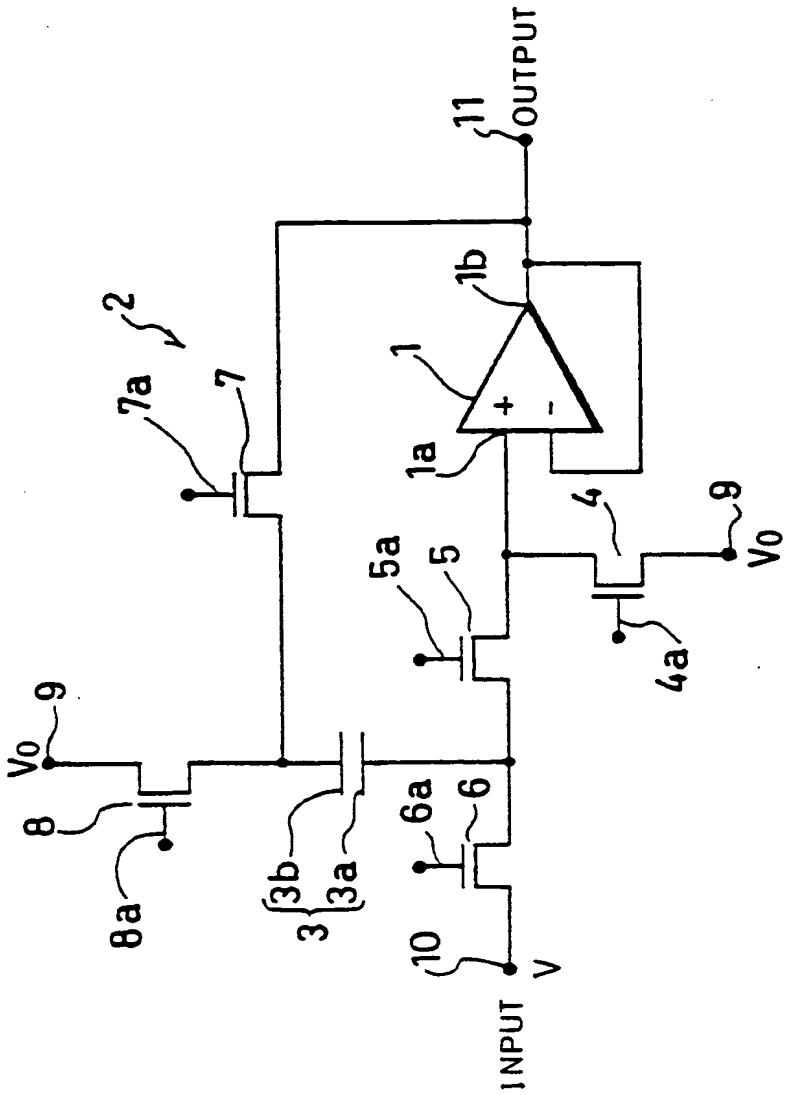


FIG.4

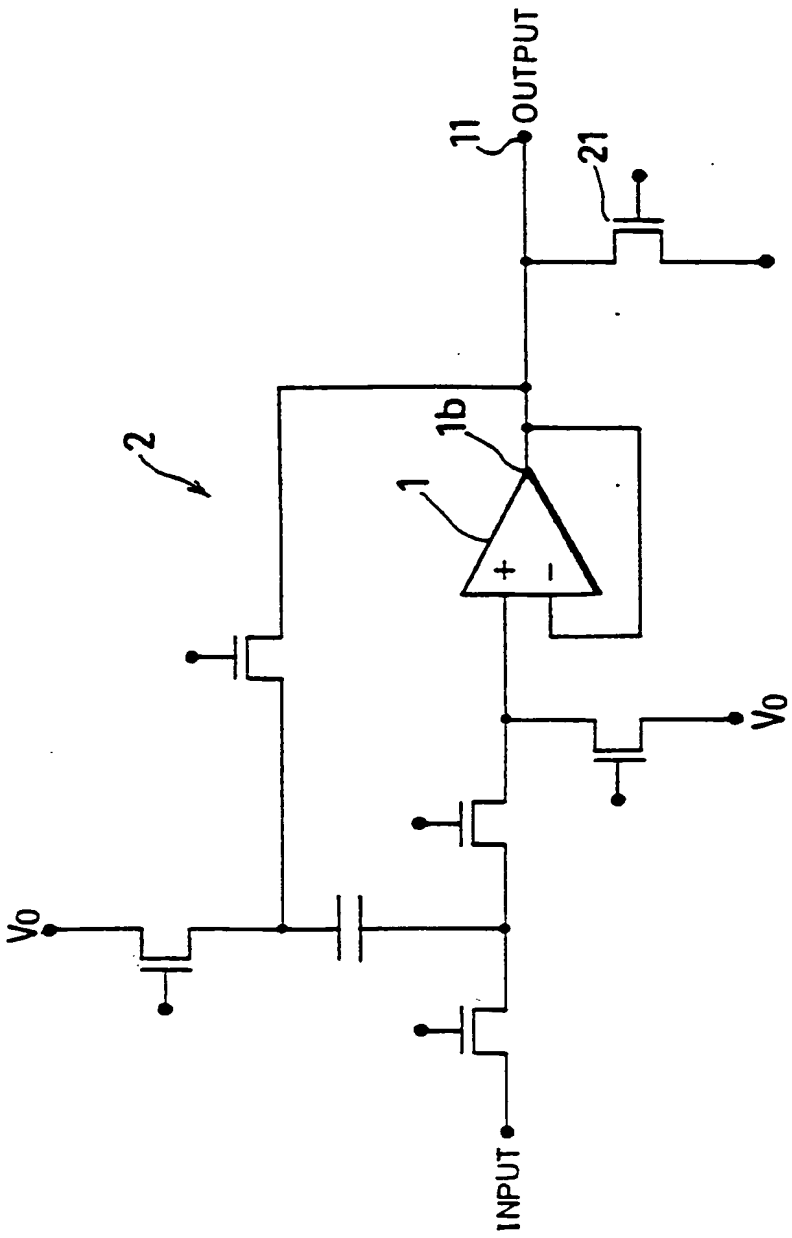


FIG. 6

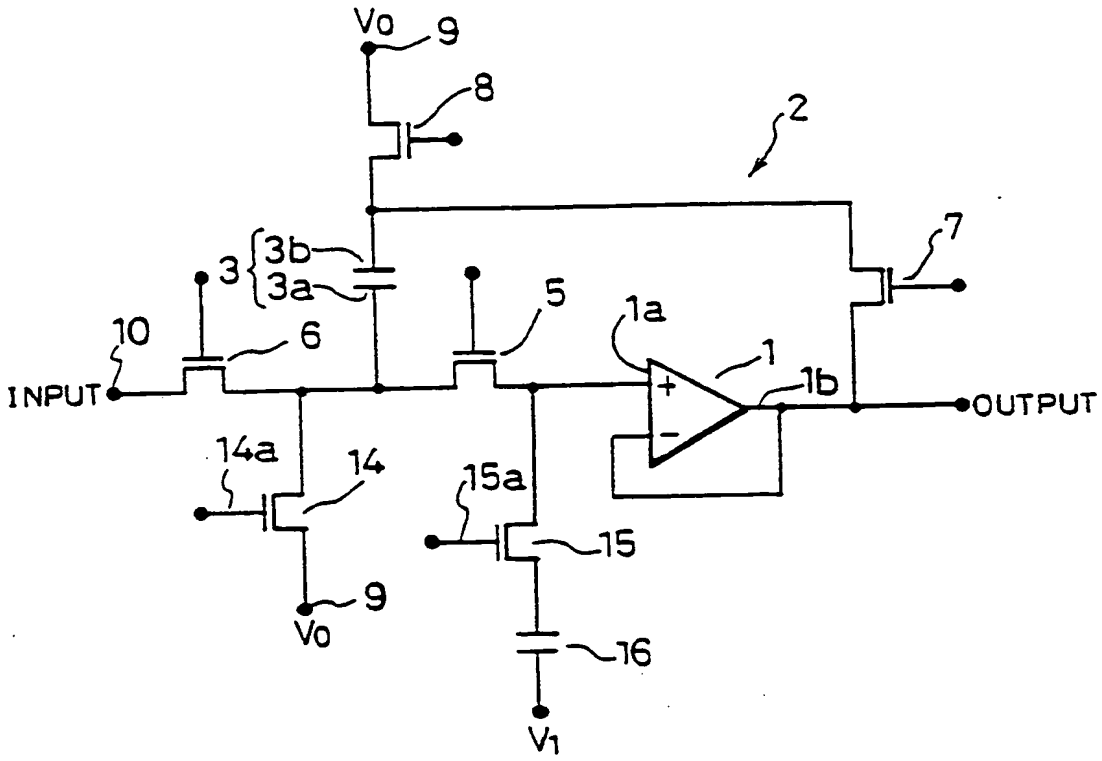
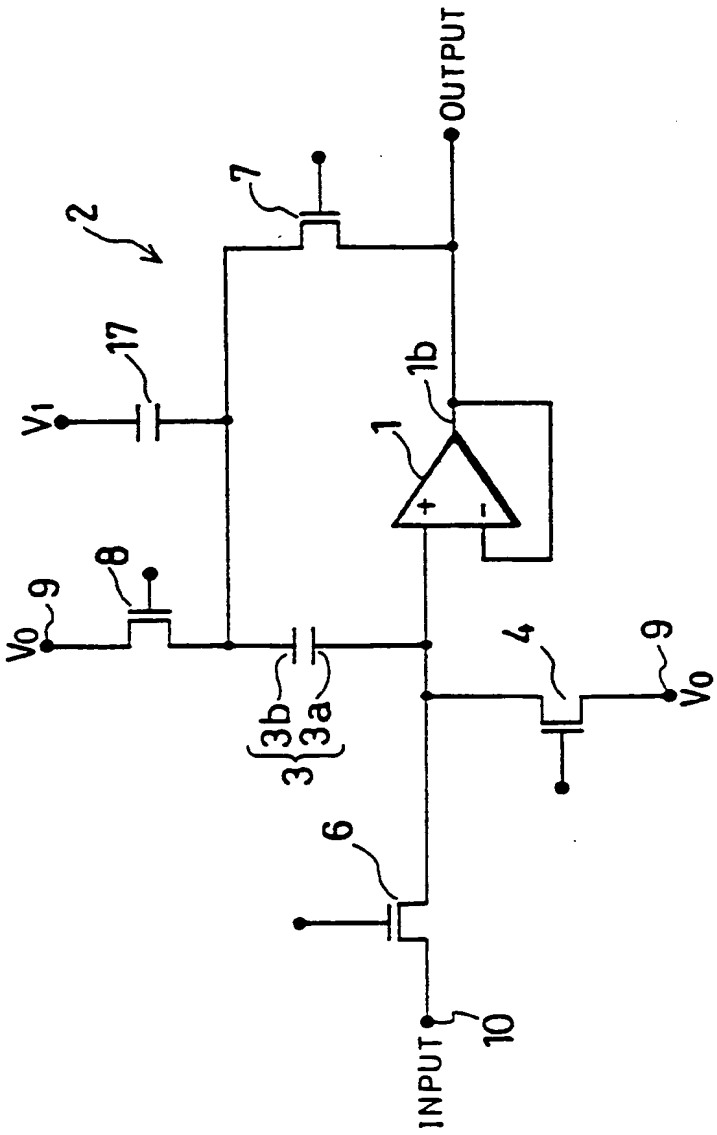


FIG.8



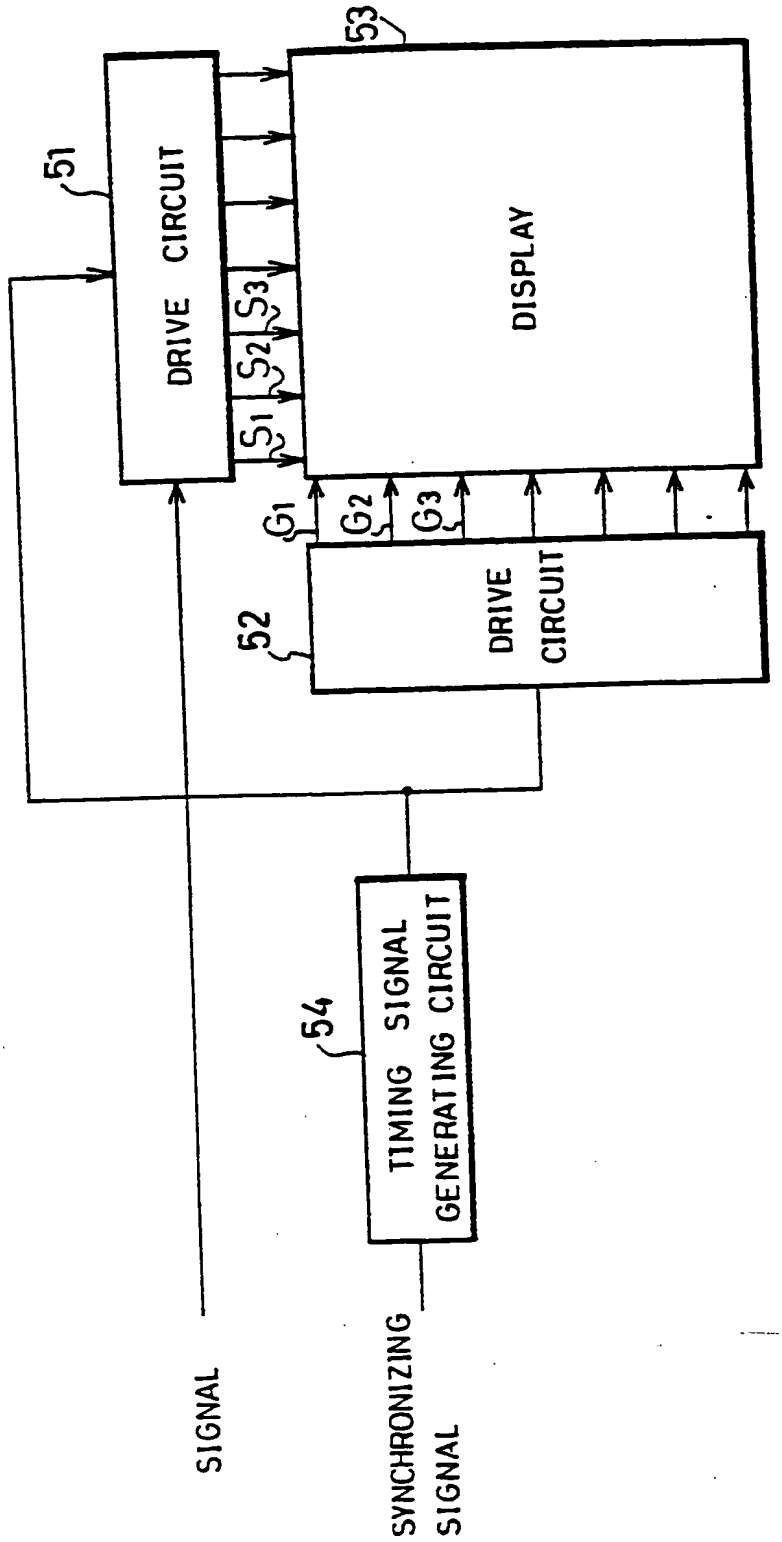

53
51
DRIVE CIRCUIT
DISPLAY
S3
S2
S1
G1
G2
G3
52
DRIVE CIRCUIT
54
TIMING SIGNAL GENERATING CIRCUIT
SIGNAL
SYNCHRONIZING SIGNAL

FIG.10

FIG.12

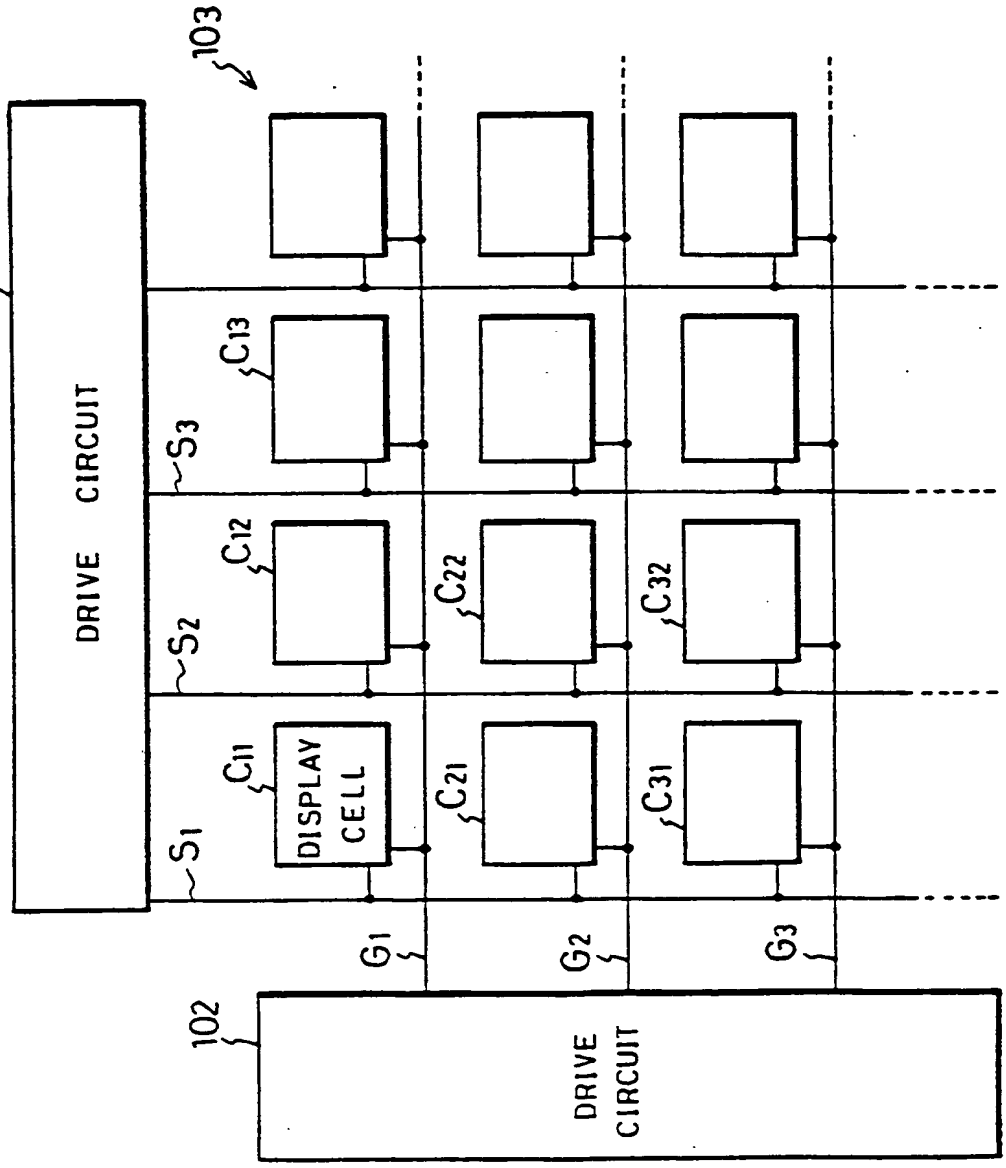

103
101
DRIVE CIRCUIT
C13
S3
C12
C22
C32
S2
C11
DISPLAY CELL
C21
C31
S1
G1
G2
G3
102
DRIVE CIRCUIT

FIG.14

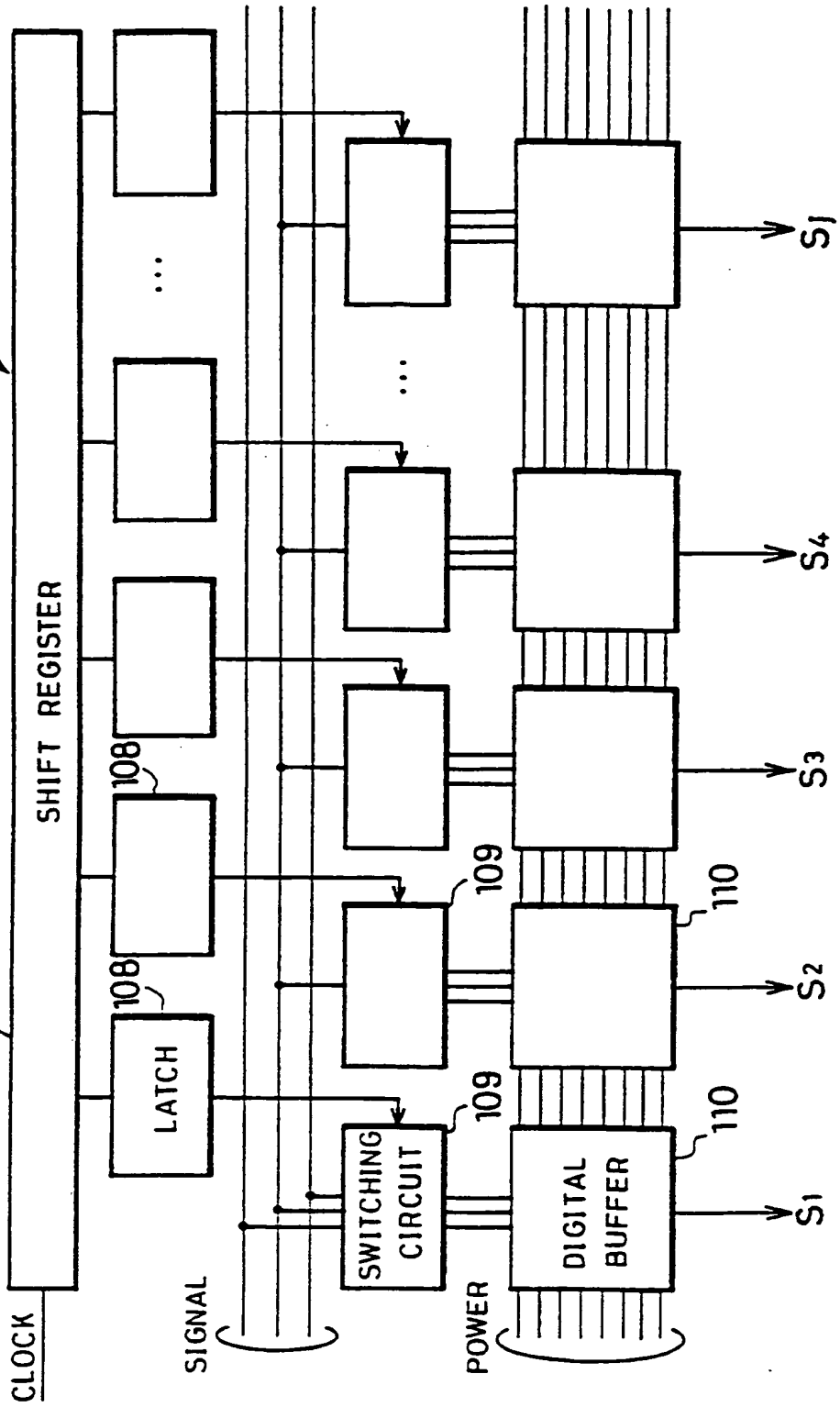

101
SHIFT REGISTER
107
CLOCK
108
LATCH
SIGNAL
109
SWITCHING CIRCUIT
POWER
110
DIGITAL BUFFER
S1
S4
S3
S2
S1

FIG.16

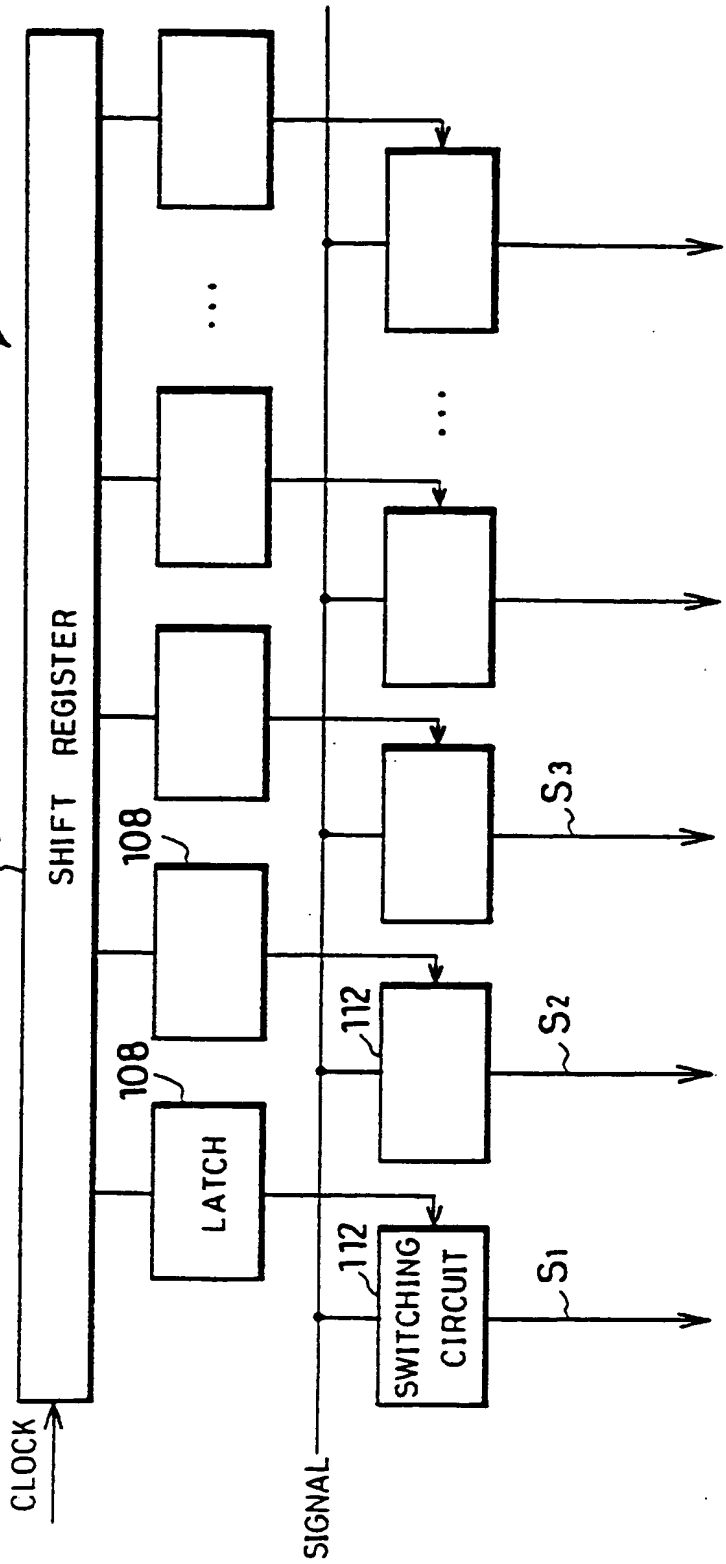

101
SHIFT REGISTER
107
108
108
LATCH
112
112
SWITCHING CIRCUIT
S3
S2
S1
CLOCK
SIGNAL

FIG. 18

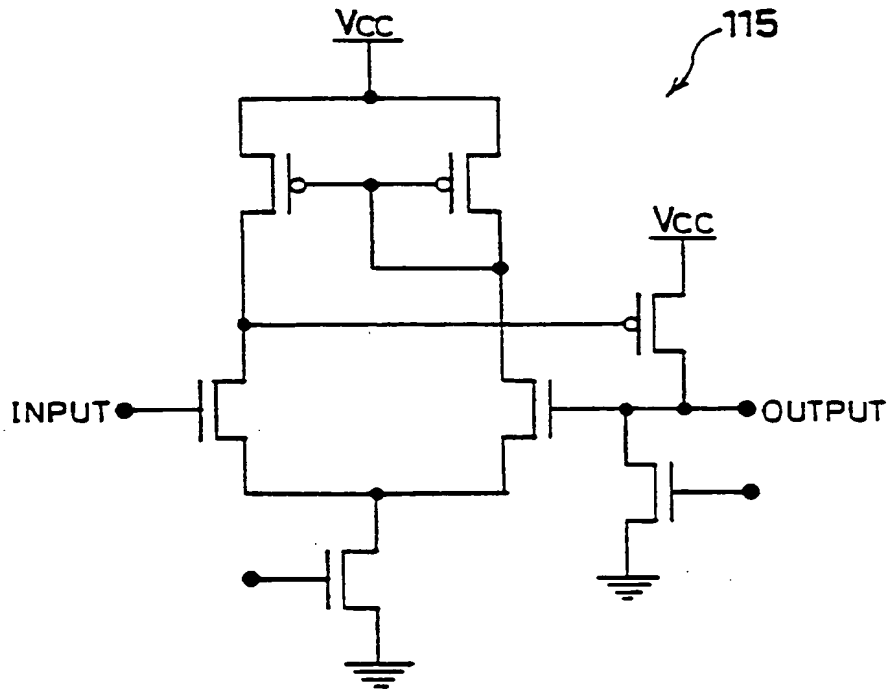


FIG. 20